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Interconnectivity

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PDIUSBD12 Evaluation Board (PC Kit)

User's Manual

Rev. 2.1

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INSTALLATION OF PDIUSBD12 EVALUATION BOARD

Introduction

The PDIUSBD12 evaluation kit uses 2 PC as a complete USB development environment, a host PC with USB host capability and a device PC running PDIUSBD12's firmware. The PDIUSBD12 ISA bridging board is plugged inside the device PC and connects to the evaluation board using a 25-wire cable. So the device PC behaves as a big USB device.

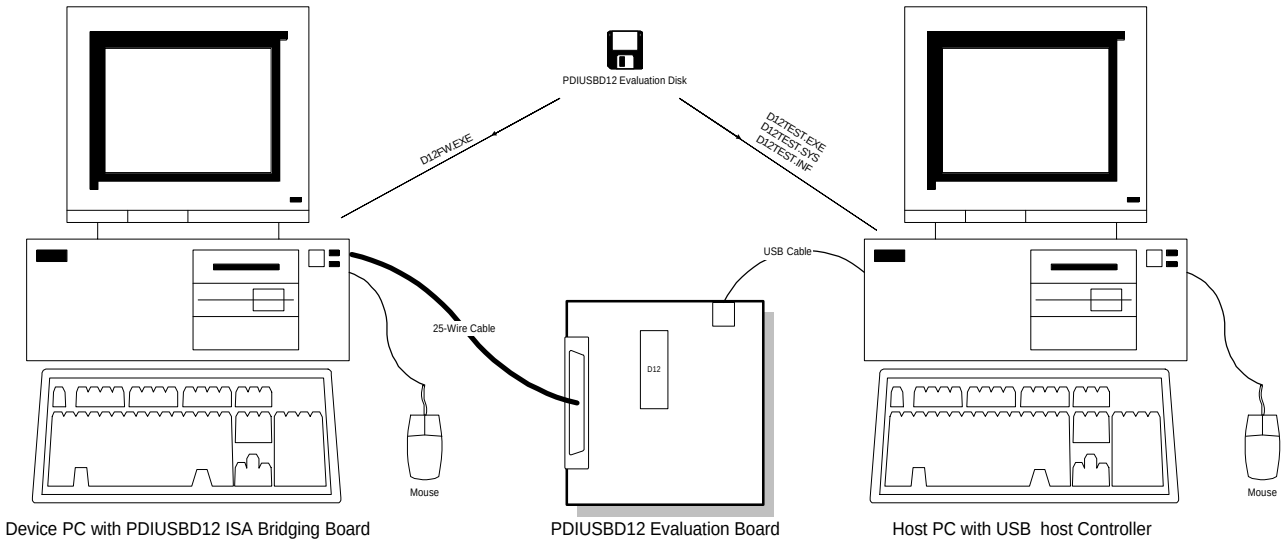
Features evaluation of PDIUSBD12, firmware and product prototype development can be easily done with this setup, without the resource limitation of a micro-controller. Customers can also connect the evaluation board to their own CPU and bus through the 25-wire cable for final product development. The firmware is carefully developed for high rate data transmission and is written in C, that supports Borland Turbo C for x86 and Keil C51 for 8031 currently. Supporting to other CPU platforms will be available soon.

System Requirements

1. PDIUSBD12 evaluation board and ISA bridging board;
2. 25-wire shielding data switch cable;
3. Host PC with USB motherboard or add-on card;
4. Microsoft Windows 98 or Windows NT 5.0 Beta 2;
5. Device PC running Microsoft DOS 6.x;
6. PDIUSBD12 evaluation diskette.

For firmware development:

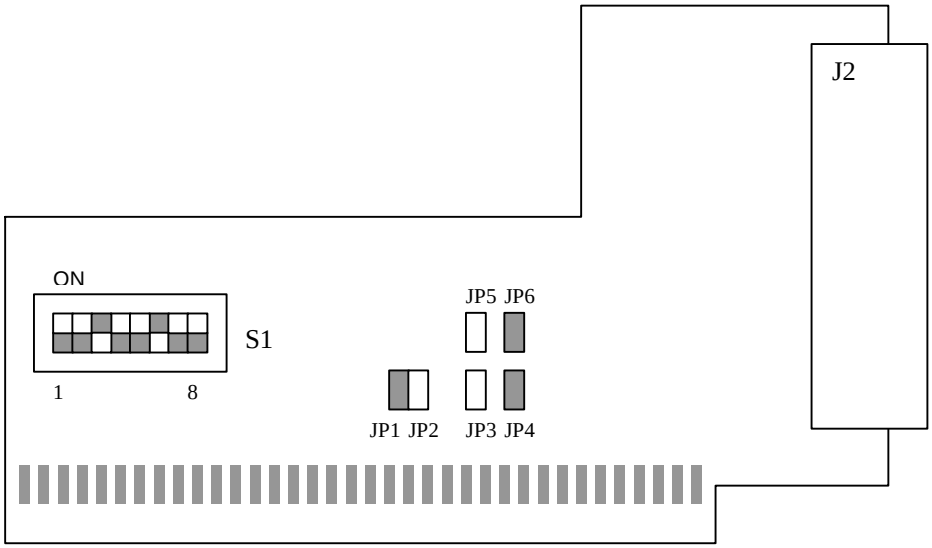
1. X86 CPU platform: Borland Turbo C++ 3.0 or above;
2. 8031: Keil C51 4.0 or above.



Installation

Jumper's setting on PDIUSBD12 ISA bridging board

The PDIUSBD12 ISA bridging board is plugged inside the device PC. It will occupy I/O, IRQ and DMA resources of the device PC. To avoid possible conflicts in settings, we suggest removal of all the unnecessary cards from the device PC. Sound card and network card may cause conflict in IRQ and DMA setting.



Switch S1 sets the base I/O address for the D12 evaluation board. Default base address is 0x368. The D12 evaluation board occupies 8 I/O locations. A0 to A2 are decoded on the D12 evaluation board. Switch S1 sets the address decoding of A3 to A9. Please notice that a switch 'ON' is logic '0'.

SW(n)	1	2	3	4	5	6	7	8
Address	X	A3	A4	A5	A6	A7	A8	A9
Default	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF

Jumpers JP1 and JP2 set the IRQ number for the D12 evaluation board. Default setting is IRQ5 or JP1 is shorted.

IRQ Number	IRQ5	IRQ7
Jumper's Setting	JP1	JP2
Default	ON	OFF

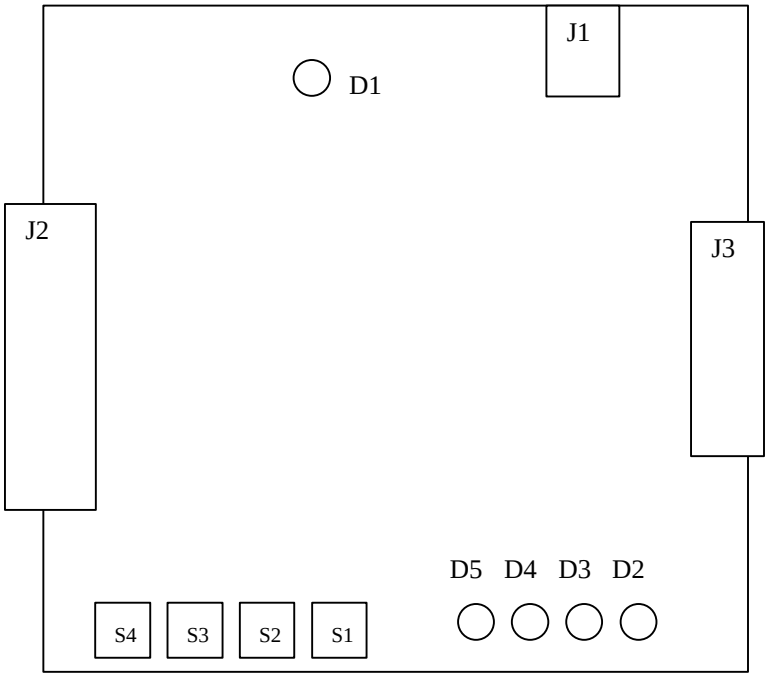
Jumpers JP3 to JP6 set the DMA number for the D12 evaluation board. Default setting is DMA3 or JP4 and JP6 are shorted. Please note that a respective pair of jumpers is needed to set a particular DMA channel.

DMA Number	DMA1	DMA3
Jumper's Setting	JP3, JP5	JP4, JP6
Default	OFF, OFF	ON, ON

Possible conflict table:

IRQ or DMA Number	Possible Conflict
IRQ5	Creative SoundBlaster™ and compatible sound cards always occupy this IRQ by default. If this kind of sound card is installed, you should check its settings or remove it. Some network cards may also use this IRQ.
IRQ7	Used by parallel port by default. May cause printing problem on device PC.
DMA1	Creative SoundBlaster™ and compatible sound cards always occupy this DMA by default. If this kind of sound card is installed, you should check its settings or remove it.
DMA3	No conflict.

Location of key components on the PDIUSBD12 evaluation board.



See the table below for the list of connectors.

Connector	Descriptions
J1	USB upstream connector
J2	DB25 data bus connector
J3	Extension board connector

See the table below for the list of switch and LEDs.

Name	Descriptions
S1, S2, S3, S4	Test switches
D1	*GoodLink*™ LED
D2, D3, D4, D5	Test LEDs

Installation of firmware, INF and driver

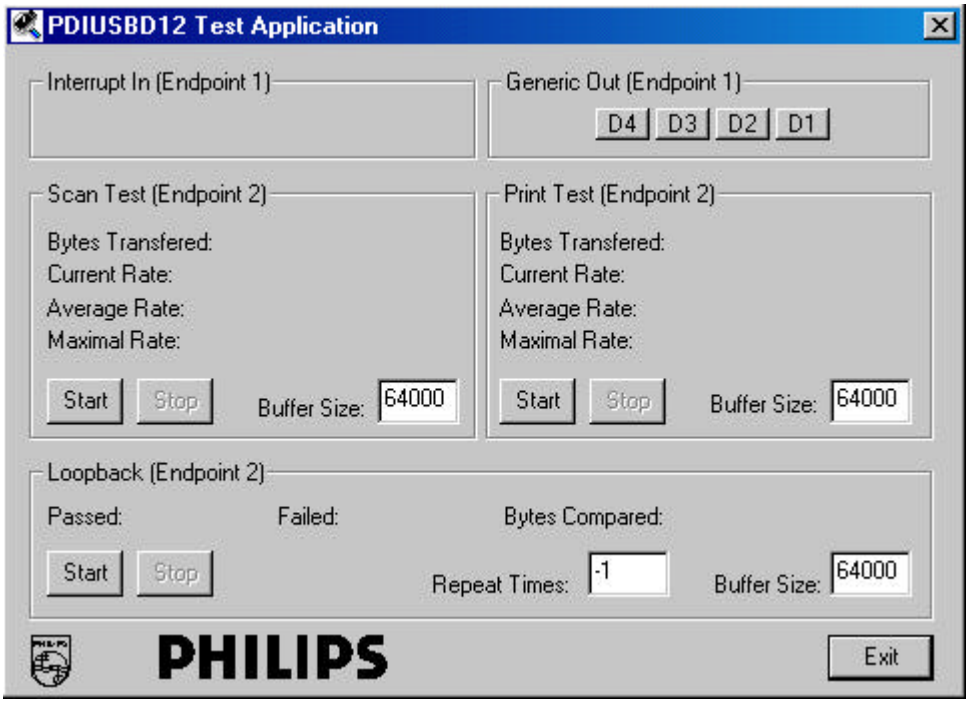
The firmware, D12FW.EXE, runs on the device PC under DOS mode. When D12FW starts, it lights up test LEDs on the evaluation board for 1 second. This means that the I/O address setting is correct. And the evaluation board is disconnected and re-connected to USB by *SoftConnect™*. If this is the first time that the evaluation board is connected to host PC, host OS Device Manager will prompt installation of INF and driver. Select the location of D12TEST.INF and D12TEST.SYS and complete installation procedure.

Some useful key command is supported when the firmware is running.

Key	Operation
ESC	Disconnect USB and quit PDIUSBD12 firmware.
ENTER	Reconnect USB using *SoftConnect™*.
i	Display firmware status information.
v	Switch on/off verbose mode, normally turned off for faster operation.

Using the Host Applet

The test applet, D12TEST.EXE, exercises all PDIUSBD12 endpoints. Testing of control endpoints can be further done by standard USB Chapter 9 test programs.



The operation of each endpoint is designed according to its nature that is supported in PDIUSBD12. Generic in and generic out endpoints has max packet size of 16 bytes and supports I/O access only. So they are suitable for small size and low rate data transfer like keyboard and logic controls. The main endpoints have max packet size of 64 bytes or 128 bytes with double buffering and DMA support. So they are suitable for high data rate, large size data transfer.

See the table below for the description of endpoints operations on PDIUSBD12 evaluation board.

Endpoint Number	Endpoint Type	Operations
1	Generic In	This pipe is defined as Interrupt In pipe. The PDIUSBD12 evaluation board sends key press/release data packet to the host when test keys are pressed or released. The firmware uses I/O accesses on this endpoint.
1	Generic Out	This pipe is defined as Interrupt Out pipe. Data packet received from host is interpreted as LED control and the D12 evaluation board firmware will light up the corresponding LED. The firmware uses I/O accesses on this endpoint.
2	Main In Main Out	These pipes are defined as Bulk In/Out endpoints. Test applet and the PDIUSBD12 evaluation board supports 3 test modes: loop-back mode, print mode and scan mode. The firmware uses DMA for data transfer on these endpoints.

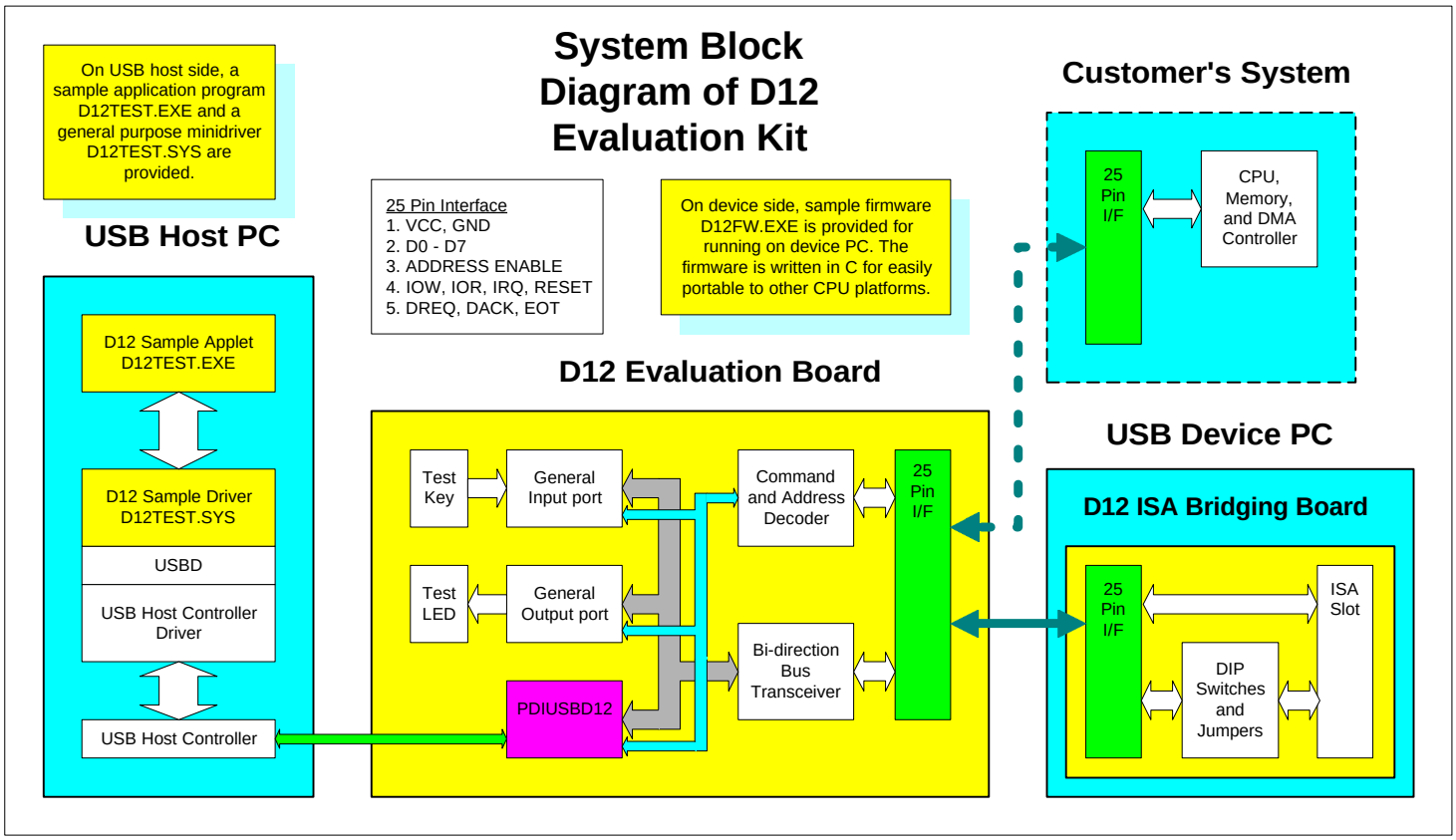
Main endpoints support 3 different test modes:

1. Scan mode: The PDIUSBD12 evaluation board acts like a scanner. It sends data packets to the host PC as fast as possible. This mode is used to evaluate the maximal Bulk In transfer rate.
2. Print mode: The PDIUSBD12 evaluation board acts like a printer. It receives data packets from the host PC as fast as possible. This mode is used to evaluate the maximal Bulk Out transfer rate.
3. Loop back mode: In this mode, the PDIUSBD12 evaluation board receives data packets on Main Out endpoint and sends them back to the host PC on Main In endpoint. This mode is used to test the data integrity of transfers.

The "Buffer Size" setting on the test applet is determined by the firmware and hardware ability of the evaluation board. For PC kit, the maximal size is limited to 64000; On USB-EPP kit, this is limited to 16384.

The "Repeat Times" for loop-back test controls the numbers of iterations of loop-back, which is useful for debugging. "-1" means it is infinite.

HARDWARE DESCRIPTION



Block Diagram

Above block diagram shows 5 main components on the PDIUSBD12 evaluation board. Beside bus transceiver, address/command decoder and PDIUSBD12, a general input port and a general output port are included in the design. These input and output ports are designed for test purposes, such as test switches and test LEDs. They also act as glue logic to adapt the PDIUSBD12 to the ISA bus. For example, ISA interrupt is edge triggered, but PDIUSBD12 interrupt is level triggered. The MSB of the general output port is used as interrupt enable to convert level triggered interrupt to edge triggered.

I/O Mapping

PDIUSBD12 evaluation board uses 8 I/O addresses:

Offset	Usage
0	D12 data register, R/W
1	D12 command register, W only
2	General input port, R only
3	General output port, W only
4 to 7	Reserved for expansion board

Bit description for general input port:

Bit	Usage
0	Key S1, '0' for pressed
1	Key S2, '0' for pressed
2	Key S3, '0' for pressed
3	Key S4, '0' for pressed
4	D12 *GoodLink*™ pin state
5	USB bus power state, '1' for USB VBUS present
6	D12 SUSPEND pin state
7	D12 INT_N pin state

Bit description for general output port:

Bit	Usage
0	LED D2, '1' lights up LED
1	LED D3, '1' lights up LED
2	LED D4, '1' lights up LED
3	LED D5, '1' lights up LED
4	Reserved
5	Reserved
6	Suspend control, '1' forces D12 SUSPEND pin low
7	Interrupt enable, '1' enables interrupt

Connectors

25 wire connector for PDIUSBD12 evaluation board:

Pin	Type	Description
1	POWER	VCC
2	POWER	GND
3	I/O	DATA7
4	I/O	Zero Wait State
5	I/O	DATA6
6	I/O	Reserved
7	I/O	DATA5
8	O	CLKOUT: This line is connected to PDIUSBD12 CLKOUT pin.
9	I/O	DATA4
10	I	-AD_EN: This line is the decoder output for address decoding A3 to A9. This signal is active low when PDIUSBD12 evaluation board I/O address is selected.
11	I/O	DATA3
12	I	RESET: This line is used to reset or initialize system logic upon power-up and is active high.
13	I/O	DATA2
14	I	-IOW: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
15	I/O	DATA1
16	I	-IOR: This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

17	I/O	DATA0
18	I	T/C, Terminal Count: This line provides a pulse when terminal count for any DMA channel is reached. This signal is active high.
19	I	ADDR2
20	I	-DACK: This line is used to acknowledge DMA request and is active low.
21	I	ADDR1
22	O	DRQ: This line is asynchronous channel request used by peripheral devices to gain DMA service. A DMA request is generated by bringing DRQ line to an active high.
23	I	ADDR0
24	O	IRQ: This line is raising edge triggered. An interrupt request is generated by raising this line high and hold until it is acknowledged by the processor.
25	POWER	GND

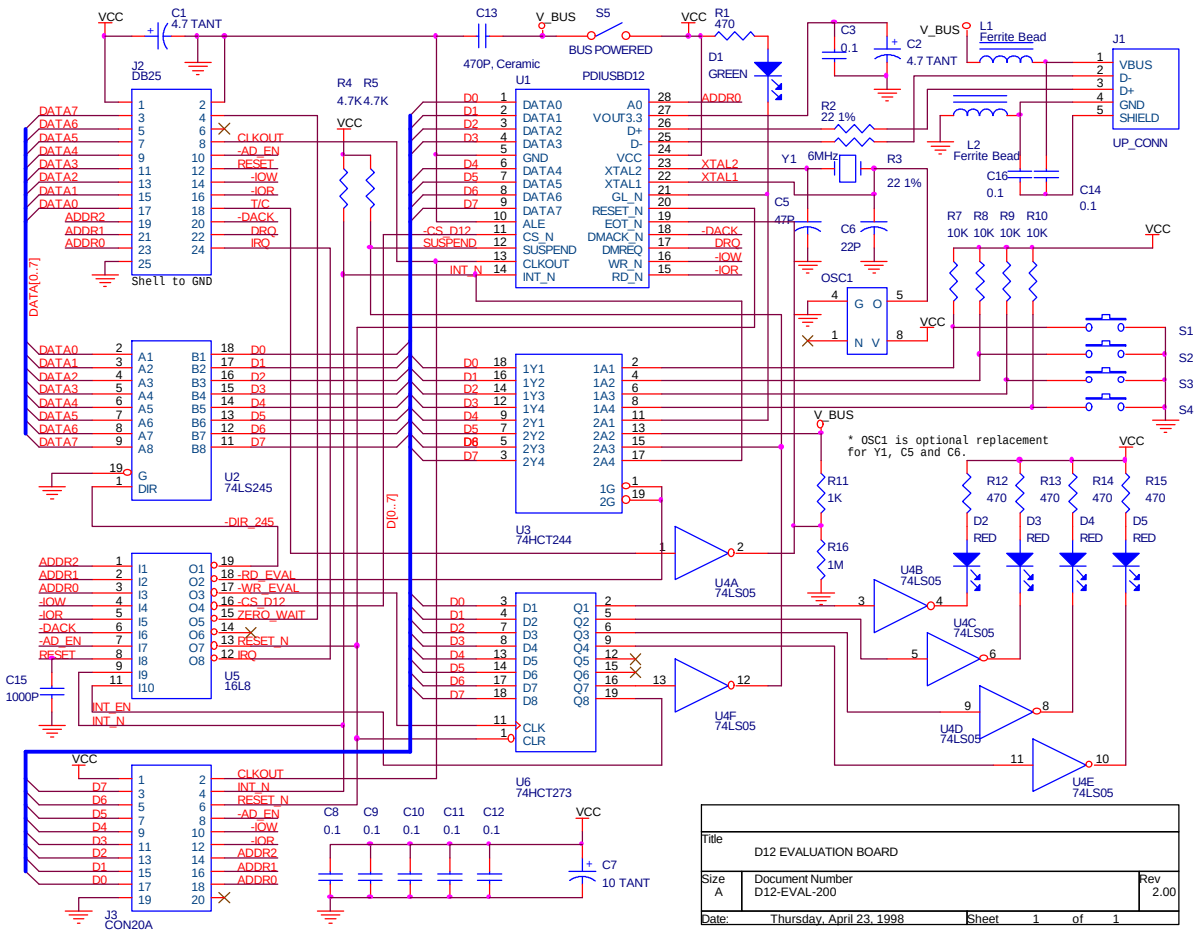
PAL Equations

Address and command decoder

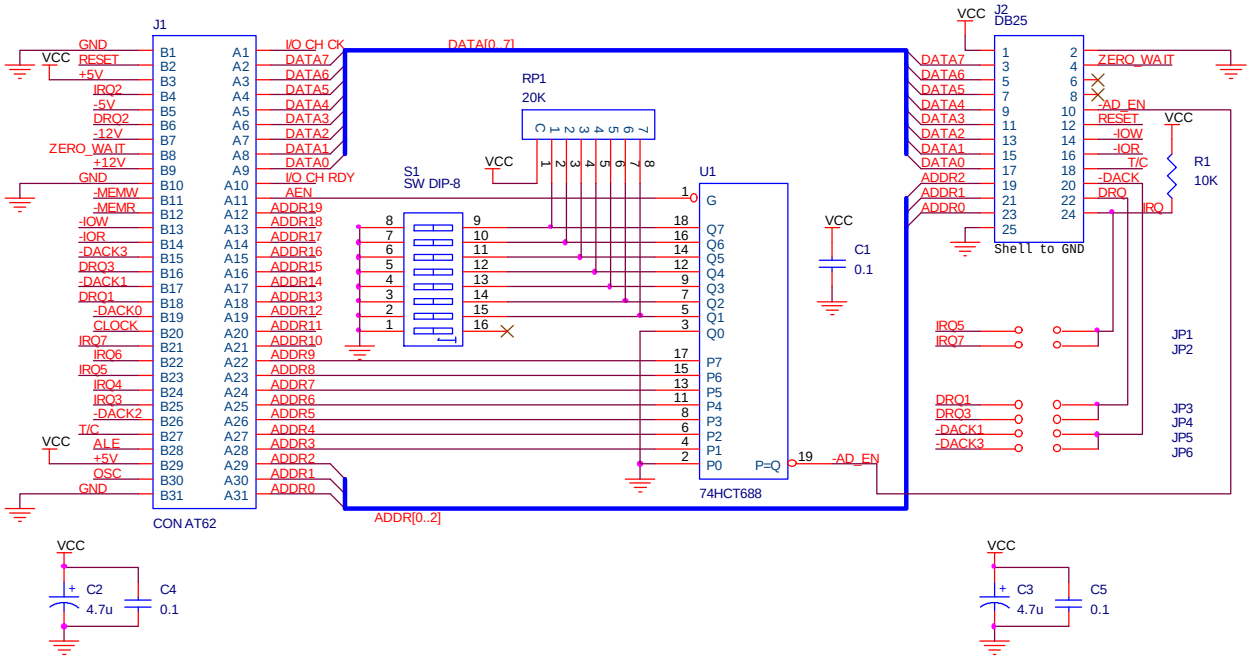
```
/**  Inputs  **/

Pin 1 = ADDR2;
Pin 2 = ADDR1;
Pin 3 = ADDR0;
Pin 4 = !IOW;
Pin 5 = !IOR;
Pin 6 = !DACK;
Pin 7 = !AD_EN;
Pin 8 = RESET;
Pin 9 = INT_N;
Pin 11 = INT_EN;

/**  Outputs  **/

Pin 12 = IRQ;
Pin 13 = RESET_N;
Pin 14 = RD_N;
Pin 15 = WAIT;
Pin 16 = !CS_D12;
Pin 17 = !WR_273;
Pin 18 = !RD_244;
Pin 19 = !DIR_245;

/**  Logic Equations  **/

!DIR_245 = (!AD_EN & !DACK) # !IOR # RESET;
!RD_244 = !AD_EN # !(!ADDR2 & ADDR1 & !ADDR0) # !IOR;
!WR_273 = !AD_EN # !(!ADDR2 & ADDR1 & ADDR0) # !IOW;
!CS_D12 = !AD_EN # !(!ADDR2 & !ADDR1) # (!IOW & !IOR);
RESET_N = !RESET;
IRQ = !INT_N & INT_EN;
WAIT.OE = CS_D12;
WAIT = RESET;
RD_N = !IOR;
```

Schematics

Schematics for PDIUSBD12 evaluation board



Schematic for PDIUSBD12 ISA bridging board



Title	D12 ISA BRIDGING BOARD		
Size A	Document Number D12-ISA-200		Rev 2.00
Date: Tuesday, February 24, 1998	Sheet 1 of 1		

Bill of Materials

Bill of materials of the PDIUSBD12 evaluation board

Item	Quantity	Reference	Part
1	2	C2,C1	4.7 TANT
2	8	C3,C8,C9,C10,C11,C12,C14,C16	0.1
3	1	C5	47P
4	1	C6	22P
5	1	C7	10 TANT
6	1	C13	470P, Ceramic
7	1	C15	1000P
8	1	D1	GREEN
9	4	D2,D3,D4,D5	RED
10	1	J1	UP_CONN
11	1	J2	DB25
12	1	J3	CON20A
13	2	L1,L2	Ferrite Bead
14	1	OSC1	Crystal Oscillator
15	5	R1,R12,R13,R14,R15	470
16	2	R2,R3	22 1%
17	2	R4,R5	4.7K
18	4	R7,R8,R9,R10	10K
19	1	R11	1K
20	1	R16	1M
21	4	S1,S2,S3,S4	SW PUSHBUTTON
22	1	S5	BUS POWERED
23	1	U1	PDIUSBD12
24	1	U2	74LS245
25	1	U3	74HCT244
26	1	U4	74LS05
27	1	U5	16L8
28	1	U6	74HCT273
29	1	Y1	6MHz

Bill of materials of the PDIUSBD12 ISA bridging board

Item	Quantity	Reference	Part
1	3	C1,C4,C5	0.1
2	2	C2,C3	4.7u
3	6	JP1,JP2,JP3,JP4,JP5,JP6	JUMPER
4	1	J1	CON AT62
5	1	J2	DB25
6	1	RP1	20K
7	1	R1	10K
8	1	S1	SW DIP-8
9	1	U1	74HCT688